REMARKS

The following remarks supplement the remarks provided as part of the response filed November 16, 2004, and are provided so as to address the Examiner's concerns with regard to the Amendment filed November 16, 2004 being non-responsive.

While Applicants' admitted prior art as described in the original specification may be construed to include a positioning mechanism for aligning a reference position of a polished and cleaned semiconductor wafer with a predetermined direction, this prior art does not disclose or suggest an apparatus including a support member from which a polished and cleaned semiconductor wafer is to received by the positioning mechanism, with the support member

> **having a tapered surface for contacting a circumferential edge of the polished and cleaned semiconductor wafer such that the polished and cleaned semiconductor wafer becomes centered,**

as recited in independent claims 5 and 16. As such, this admitted prior art also does not disclose the polishing method as recited in independent claim 13, which method includes

> **centering said polished and cleaned semiconductor wafer by contacting a circumferential edge of said polished and cleaned semiconductor wafer with a tapered surface of a support member... from said support member, receiving said polished and cleaned semiconductor.**

Thus, each of independent claims 5, 13 and 16 is not anticipated by Applicants' admitted prior art, whereby claims 5-7, 13, 14, 16 and 19-31 are allowable over Applicant's admitted prior art.

Similarly, while robot 2 of Oishi et al. may possibly be said to correspond to a positioning mechanism for aligning a reference position of a polished and cleaned semiconductor wafer with a predetermined direction, Oishi et al. does not disclose or suggest an apparatus including a support

member from which a polished and cleaned semiconductor wafer is to received by the robot 2, with the support member

> **having a tapered surface for contacting a circumferential edge of the polished and cleaned semiconductor wafer such that the polished and cleaned semiconductor wafer becomes centered,**

as recited in independent claims 5 and 16. As such, Oishi et al. also does not disclose the polishing method as recited in independent claim 13, which method includes

> **centering said polished and cleaned semiconductor wafer by contacting a circumferential edge of said polished and cleaned semiconductor wafer with a tapered surface of a support member... from said support member, receiving said polished and cleaned semiconductor.**

Thus, each of independent claims 5, 13 and 16 is not anticipated by Oishi et al., whereby claims 5-7, 13, 14, 16 and 19-31 are allowable over Oishi et al.

Similarly, while JP '241 may disclose a positioning mechanism for aligning a reference position of a polished and cleaned semiconductor wafer with a predetermined direction, JP '241 does not disclose or suggest an apparatus including a support member from which a polished and cleaned semiconductor wafer is to received by this positioning mechanism, with the support member

> **having a tapered surface for contacting a circumferential edge of the polished and cleaned semiconductor wafer such that the polished and cleaned semiconductor wafer becomes centered,**

as recited in independent claims 5 and 16. As such, JP '241 also does not disclose the polishing method as recited in independent claim 13, which method includes

> **centering said polished and cleaned semiconductor wafer by contacting a circumferential edge of said polished and cleaned semiconductor wafer with a tapered surface of a support member... from said support member, receiving said polished and cleaned semiconductor.**

Thus, each of independent claims 5, 13 and 16 is not anticipated by JP '241., whereby claims 5-7, 13, 14, 16 and 19-31 are allowable over JP '241.

Similarly, while robot 10 of Okumura et al. may possibly be said to correspond to a positioning mechanism for aligning a reference position of a polished and cleaned semiconductor wafer with a predetermined direction, Okumura et al. does not disclose or suggest an apparatus including a support member from which a polished and cleaned semiconductor wafer is to received by this robot, with the support member

> **having a tapered surface for contacting a circumferential edge of the polished and cleaned semiconductor wafer such that the polished and cleaned semiconductor wafer becomes centered,**

as recited in independent claims 5 and 16. As such, Okumura et al. also does not disclose the polishing method as recited in independent claim 13, which method includes

> **centering said polished and cleaned semiconductor wafer by contacting a circumferential edge of said polished and cleaned semiconductor wafer with a tapered surface of a support member... from said support member, receiving said polished and cleaned semiconductor.**

Thus, each of independent claims 5, 13 and 16 is not anticipated by Okumura et al., whereby claims 5-7, 13, 14, 16 and 19-31 are allowable over Okumura et al.

Because each of the four references relied upon by the Examiner lacks a feature of each of the independent claims, as expressed above, any combination of these references would not result in the invention as recited in any of independent claims 5, 13 and 16, whereby none of claims 5-7, 13, 14, 16 and 19-31 is obvious over a combination of any of these references. Thus, claims 5-7, 13, 14, 16 and 19-31 are allowable.

This Response has pointed out the specific distinctions of the independent claims that are believed to render these claims patentable over any of the applied references, either taken alone or in combination. Thus, this supplemental response coupled with the reply filed November 16, 2004, is fully responsive to the Office Action mailed August 16, 2004.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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